+2.5 V to +5.5 V, 140µA, 2-Wire Serial Input, Voltage Output 8/10/12-Bit DACs

Prelim Technical Information

AD5301/11/21

FEATURES

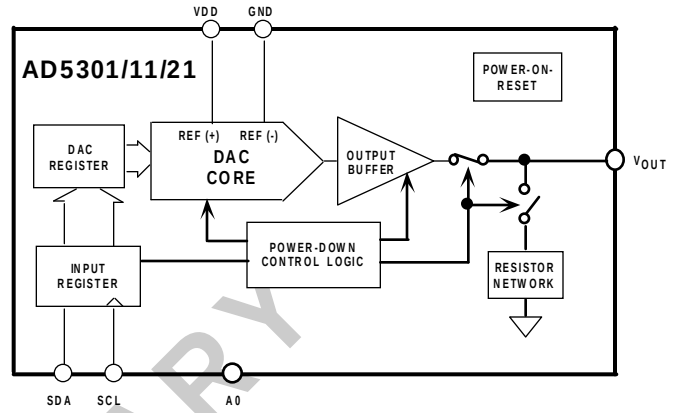
AD5301: Single 8-Bit DAC
AD5311: Single 10-Bit DAC
AD5321: Single 12-Bit DAC
6 Pin SOT-23 and 8-pin microSOIC Packages
Micropower Operation: 140µA @ 5V (including Reference Current)
Power Down to 200nA @ 5V, 50nA @ 3V
+2.5V to +5.5V Operation
Guaranteed Monotonic by Design
Reference derived from Power Supply
Power-On-Reset to Zero Volts
2-Wire Serial Interface
On-Chip Output Buffer Amplifier, Rail-to-Rail Operation

APPLICATIONS

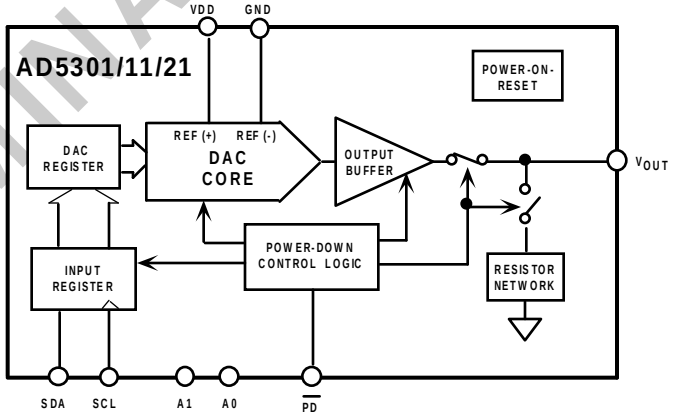
Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

FUNCTIONAL BLOCK DIAGRAM

6-Lead SOT-23



8-Lead MicroSOIC



GENERAL DESCRIPTION

The AD5301/11/21 are single 8, 10 and 12-bit buffered voltage out DACs which operate from a single +2.5V to +5.5V supply. Their on-chip precision output amplifiers allow rail-to-rail output swing to be achieved. The AD5301/11/21 utilize a 2-wire serial interface which operates at clock rates up to 400kHz. This simple interface allows communication between multiple devices on a single bus. The AD5301/11/21 contain A0 and A1 pins which allow the 2 LSBs of the 7-bit slave address to be set by the user. The first six bits have been factory programmed and are always 000110 for the 6-pin package. The first five bits are programmed as 00011 for the 8-pin package.

The reference for the AD5301/11/21 is derived from the power supply inputs and thus gives the widest dynamic output range. The parts incorporate a power-on-reset circuit that ensures that the DAC outputs power up to zero volts and remain there until a valid write takes place to the device. The parts contain a power-down feature which reduces the current consumption of to 50nA @ 3V. The parts are put into power-down mode over the serial interface with an extra option of a hardware power-down using the PD pin in the 8-pin versions.

The low power consumption of these parts in normal operation makes them ideally suited to portable battery-operated equipment. The power consumption is 0.7mW at 5V reducing to 1µW in power-down mode.

PRODUCT HIGHLIGHTS

1. Low-power, single-supply operation. These parts operate from a single +2.5V to +5.5V supply and consume typically 0.35mW at 3V and 0.7mW at 5V making them ideal for battery-powered applications.
2. The on-chip output buffer amplifiers allow the outputs of the DACs to swing rail-to-rail with a slew rate of 1V/µs.
3. Reference derived from the power supply.
4. 2-Wire serial interface with clock speeds up to 400kHz.
5. Power-down capability. When powered down the DAC consume 50nA at 3V and 200nA at 5V.
6. Packaged in 6-pin SOT-23 and in 8-Lead MicroSOIC packages.

Prelim.H1 8/98

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AD5301/11/21–SPECIFICATIONS

(V_{DD} = +2.5V to +5.5 V; R_L=2kΩ to GND; C_L=200pFto GND; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Version[1] Min	Typ	Max	Units	Conditions/Comments
DC PERFORMANCE					
AD5301					
Resolution	8			Bits	
Relative Accuracy		±0.25	±1	LSB	Output Unloaded
Differential Nonlinearity			±0.25	LSB	Output Unloaded. Guaranteed Monotonic by design
AD5311					
Resolution	10			Bits	
Relative Accuracy		±1	±3	LSB	Output Unloaded
Differential Nonlinearity			±0.5	LSB	Output Unloaded. Guaranteed Monotonic by design
AD5321					
Resolution	12			Bits	
Relative Accuracy		±4	±10	LSB	Output Unloaded
Differential Nonlinearity			±1	LSB	Output Unloaded. Guaranteed Monotonic by design
Zero Code Error			+3	LSB	Output Unloaded. All 0s loaded to DAC register.
Fullscale Error			-3	LSB	Output Unloaded. All 1s loaded to DAC register.
Gain Error			±0.75	% of FSR	
Zero Code Error Drift[3]		-20		µV/°C	
Gain Temperature Coefficient[3]		5		ppm of FSR/°C	
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Output Voltage Settling Time					
AD5301		4	6	µs	1/4 Scale to 3/4 Scale change (40Hex to C0 Hex)
AD5311		6	8	µs	1/4 Scale to 3/4 Scale change (100Hex to 300 Hex)
AD5321		8	10	µs	1/4 Scale to 3/4 Scale change (400Hex to C00 Hex)
Slew Rate		1		V/µs	
Digital-to-Analog Glitch Impulse		20		nV-s	1 LSB change around major carry.
Digital Feedthrough		0.5		nV-s	
DC Output Impedance		1		Ω	
Short Circuit Current		50		mA	V_{DD} = +5V
		20		mA	V_{DD} = +3V
Power Up Time		2.5		µs	Coming out of Power Down Mode. V_{DD} = +5V
		5		µs	Coming out of Power Down Mode. V_{DD} = +3V
LOGIC INPUTS (A0,A1)[3]					
Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.8	V	V_{DD} = +5 V ±10%
V_{INL}, Input Low Voltage			0.6	V	V_{DD} = +3 V ±10%
V_{INL}, Input Low Voltage			0.5	V	V_{DD} = +2.5 V
V_{INH}, Input High Voltage	2.4			V	V_{DD} = +5 V ±10%
V_{INH}, Input High Voltage	2.1			V	V_{DD} = +3 V ±10%
V_{INH}, Input High Voltage	2.0			V	V_{DD} = +2.5 V
Pin Capacitance			3	pF	
LOGIC INPUTS (SCL, SDA)[3]					
V_{IH}, Input High Voltage	0.7 V_{DD}		V_{DD}+0.5	V	
V_{IL}, Input Low Voltage	-0.5		0.3 V_{DD}	V	
I_{IN}, Input Leakage Current		TBD	±1	µA	V_{IN} = 0V to V_{DD}.
V_{HYST}, Input Hysteresis	0.05 V_{DD}			V	
C_{IN}, Input Capacitance		3		pF	
LOGIC OUTPUT (SDA)[3]					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Three-State Leakage Current			±1	µA	
Three-State Output Capacitance			10	pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)					DAC active and excluding load current.
V_{DD}= +4.5V to +5.5V		140	250	µA	V_{IH} = V_{DD} and V_{IL} = GND
V_{DD}= +2.5V to +3.6V		115	200	µA	V_{IH} = V_{DD} and V_{IL} = GND
I_{DD} (Power Down)					
V_{DD} = +4.5V to +5.5V		0.2	1	µA	V_{IH} =V_{DD} and V_{IL}=GND
V_{DD} = +2.5V to +3.6V		0.05	1	µA	V_{IH} =V_{DD} and V_{IL}=GND

NOTES
[1]Temperature range: B Version: -40°C to +105°C.
[2]Linearity is tested using a reduced code range.
[3]Guaranteed by Design and Characterization, not production tested.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +2.5 V to +5.5 V . All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
F_{SCL}	400	kHz max	SCL Clock Frequency
t_1	2.5	µs min	SCL Cycle Time
t_2	0.6	µs min	t_{HIGH}, SCL High Time
t_3	1.3	µs min	t_{LOW}, SCL Low Time
t_4	0.6	µs min	$t_{HD,STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU,DAT}$, Data Setup Time
t_6[2]	0.9	µs max	$t_{HD,DAT}$, Data Hold Time
	0	µs min	
t_7	0.6	µs min	$t_{SU,STA}$, Setup Time for Repeated Start
t_8	0.6	µs min	$t_{SU,STO}$, Stop Condition Setup Time
t_9	1.3	µs min	t_{BUF}, Bus Free Time Between a STOP Condition and a START Condition.
t_{10}	300	ns max	t_R, Rise Time of both SCL and SDA when receiving
	$20 + 0.1C_b$[3]	ns min	
t_{11}	250	ns max	t_F, Fall Time of SDA when transmitting.
t_{11}	300	ns max	t_F, Fall Time of both SCL and SDA when receiving
	$20 + 0.1C_b$[3]	ns min	
C_b	400	pF max	Capacitive Load for Each Bus Line.
t_{SP}[4]	50	ns max	Pulse width of spike Suppressed.

NOTES
[1]See Figure 1.
[2]A master device must provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ min}$ of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[3]C_b is the total capacitance of one bus line in pF. t_R and t_F measured between $0.3V_{DD}$ and $0.7V_{DD}$.
[4]Input filtering on both the SCL and SDA inputs suppress noise spikes which are less than 50ns.

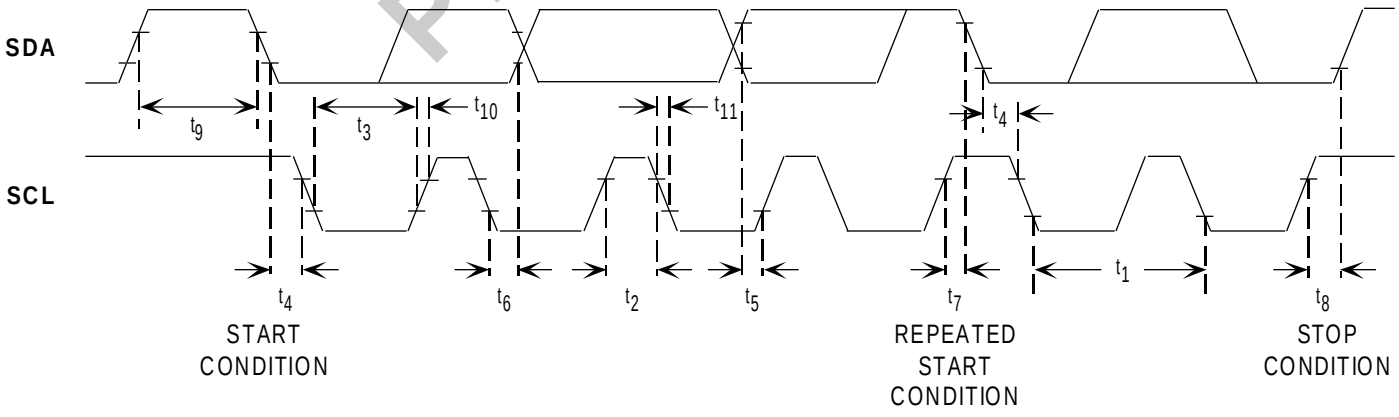


Figure 1. 2-Wire Serial Interface Timing Diagram.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND.....-0.3 V to +7 V
SCL, SDA to GND.....-0.5 V to V_{DD} + 0.5 V
A0, A1, PD to GND..... -0.3V to V_{DD} + 0.3V
V_{OUT} to GND.....-0.3V to V_{DD} + 0.3V
Operating Temperature Range
Industrial (B Version).....-40°C to +105°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature.....+150°C
SOT-23 Package
Power Dissipation.....240mW
θ_{JA} Thermal Impedance.....190°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec).....+215°C
Infrared (15 sec).....+220°C
MicroSOIC Package, Power Dissipation.....220 mW
θ_{JA} Thermal Impedance.....206°C /W
θ_{JC} Thermal Impedance.....44°C /W
Lead Temperature, Soldering
Vapor Phase (60 sec).....+215°C
Infrared (15 sec).....+220°C

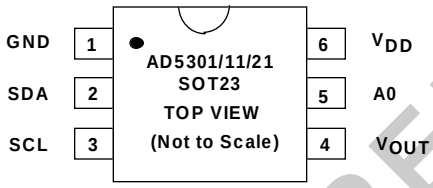
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

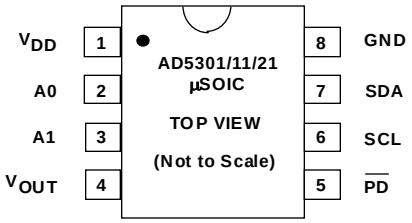
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5301/11/21 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

6-Lead SOT23



8-Lead microSOIC



PIN FUNCTION DESCRIPTION

SOT-23 PIN NUMBERS

Pin No.	Mnemonic	Function
1	GND	Ground reference point for all circuitry on the part.
2	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 16-bit input shift register. It is a bi-directional open-drain data line which should be pulled to the supply with an external pull-up resistor.
3	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 16-bit input shift register. Clock rates of up to 400kbit/s can be accommodated in the I^2C compatible interface.
4	V_{OUT}	Analog output voltage from the DAC. The output amplifier can swing rail-to-rail.
5	A0	Address Input. Sets the least significant bit of the 7-bit slave address.
6	V_{DD}	Power Supply Input. These parts can be operated from +2.5V to +5.5V and should be decoupled to GND. This supply input is also used as the reference for the DAC.

PIN FUNCTION DESCRIPTION

8-PIN MICROSOIC PIN NUMBERS

Pin No.	Mnemonic	Function
1	V_{DD}	Power Supply Input. These parts can be operated from +2.5V to +5.5V and should be decoupled to GND. This supply input is also used as the reference for the DAC.
2-3	A0, A1	Address Inputs. Sets the two least significant bits of the 7-bit slave address. (A0=LSB)
4	V_{OUT}	Analog output voltage from the DAC. The output amplifier can swing rail-to-rail.
5	$\overline{PD}$	Active Low Power-Down pin. When this pin is brought low, the part enters power-down mode.
6	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 16-bit input shift regis ter. Clock rates of up to 400kbit/s can be accommodated in the I^2C compatible interface
7	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 16-bit input shift regis ter. It is a bi-directional open-drain data line which should be pulled to the supply with an external pull-up re sistor.
8	GND	Ground reference point for all circuitry on the part.

INPUT REGISTER CONTENTS

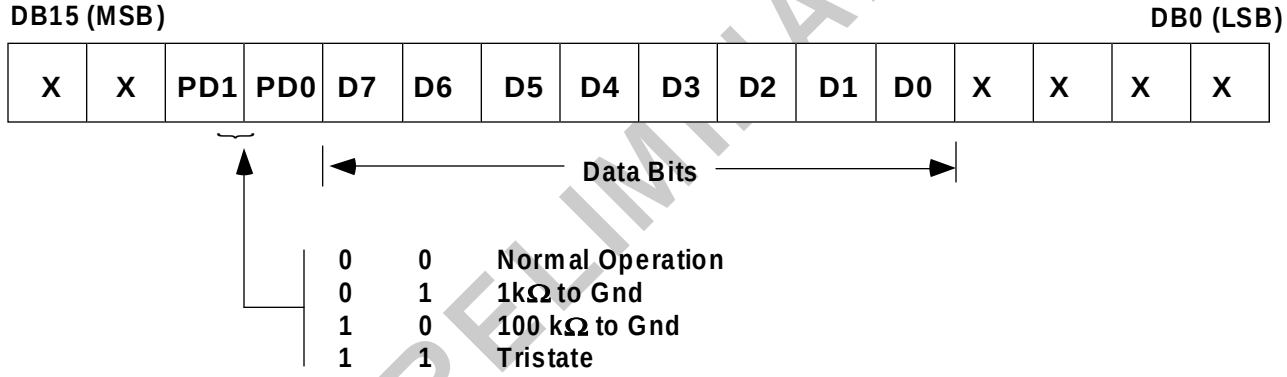


Figure 2. AD5301 Input Shift Register Contents

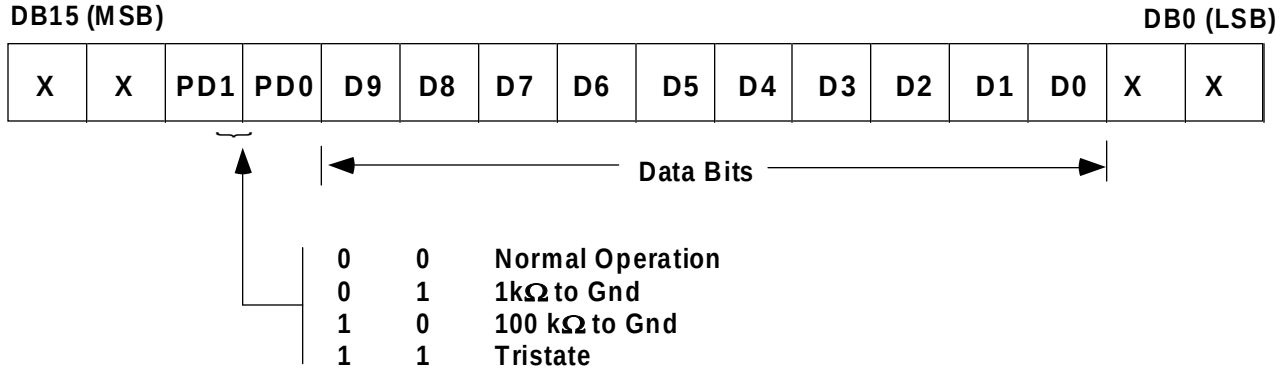


Figure 3. AD5311 Input Shift Register Contents

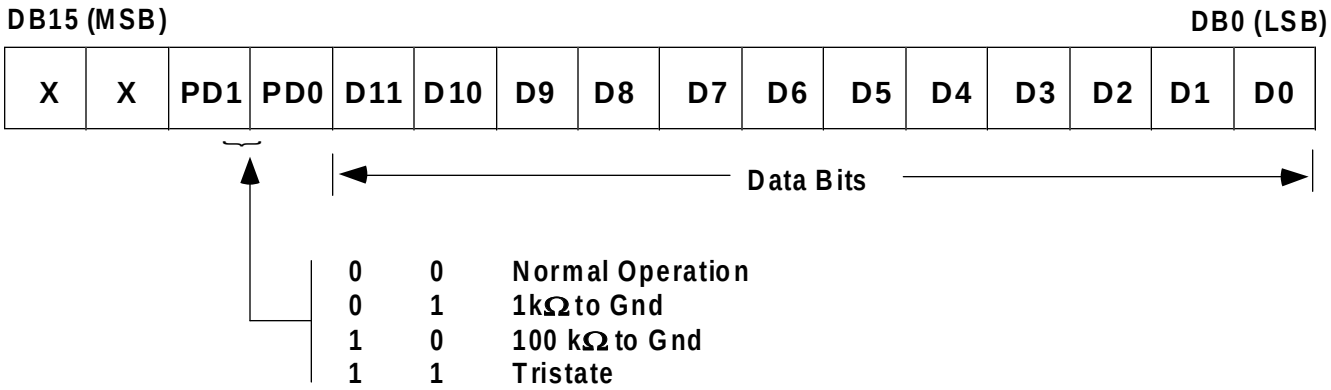
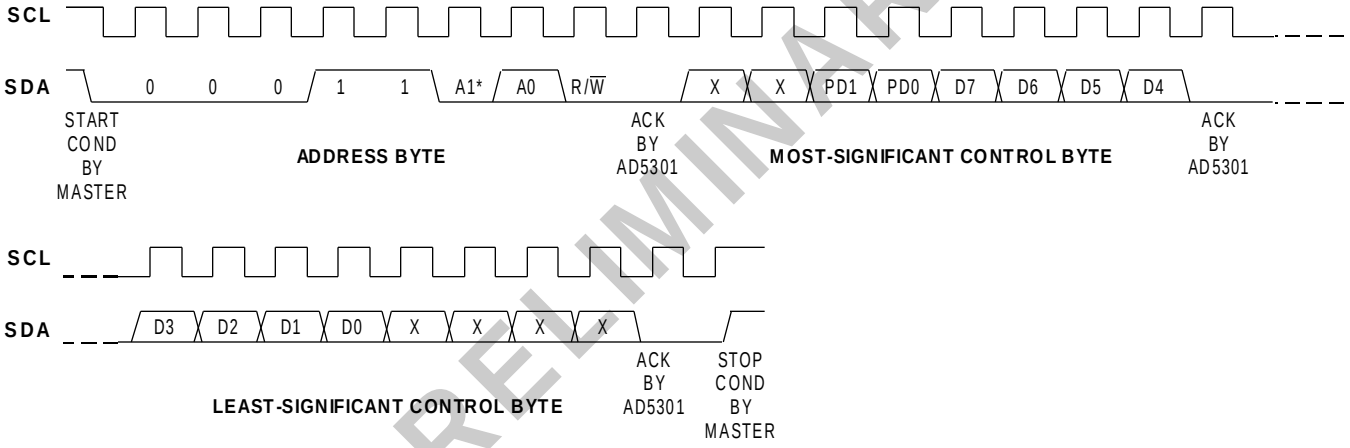


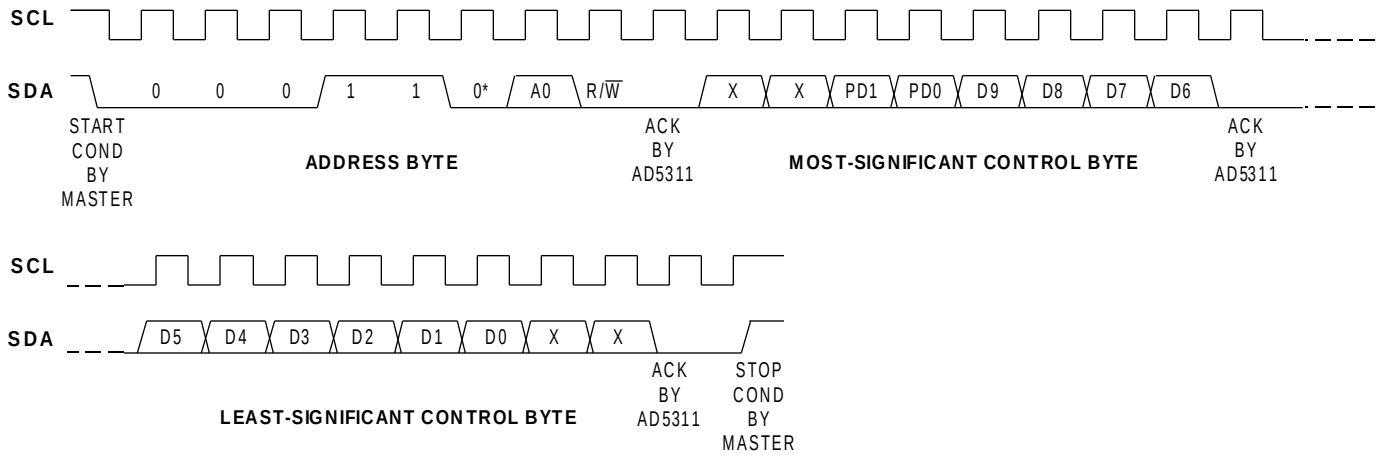
Figure 4. AD5321 Input Shift Register Contents

AD5301 WRITE SEQUENCE



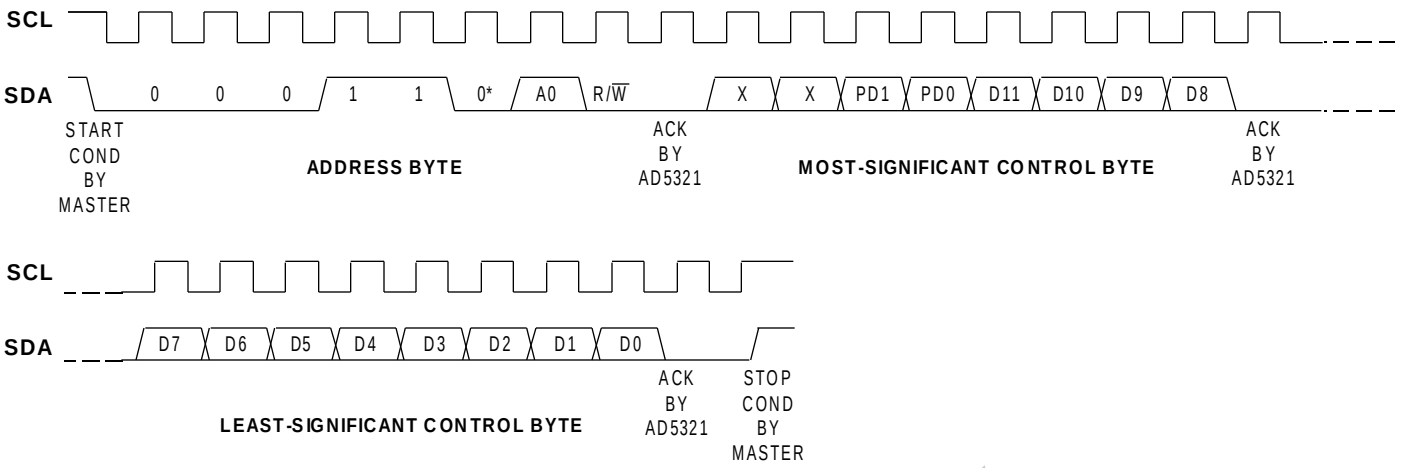
* This bit must be 0 in the 6-pin SOT23 version

AD5311 WRITE SEQUENCE



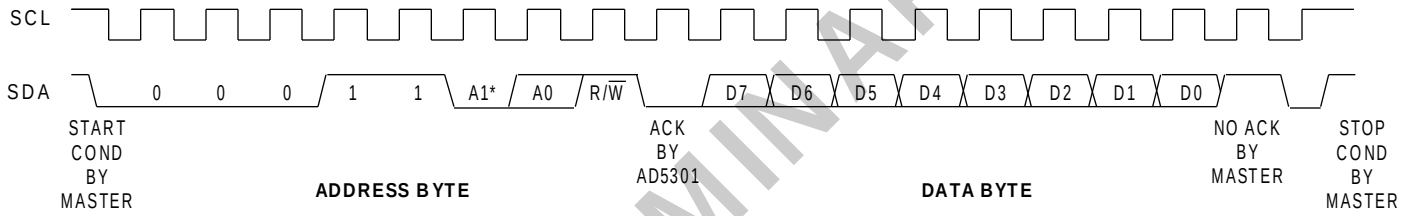
* This bit must be 0 in the 6-pin SOT23 version

AD5321 WRITE SEQUENCE



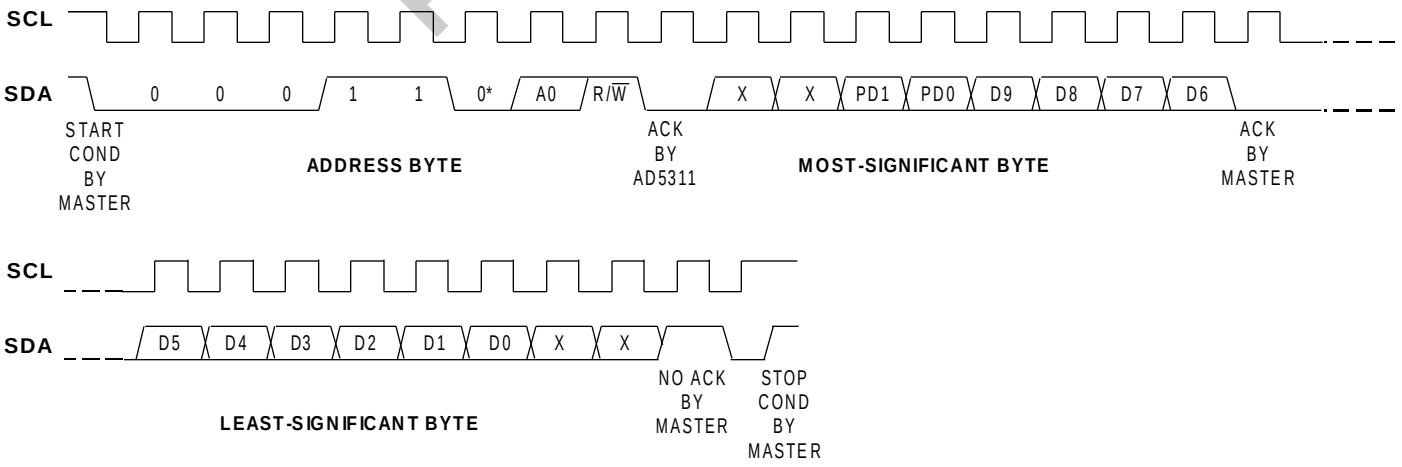
* This bit must be 0 in the 6-pin SOT23 version

AD5301 READBACK SEQUENCE



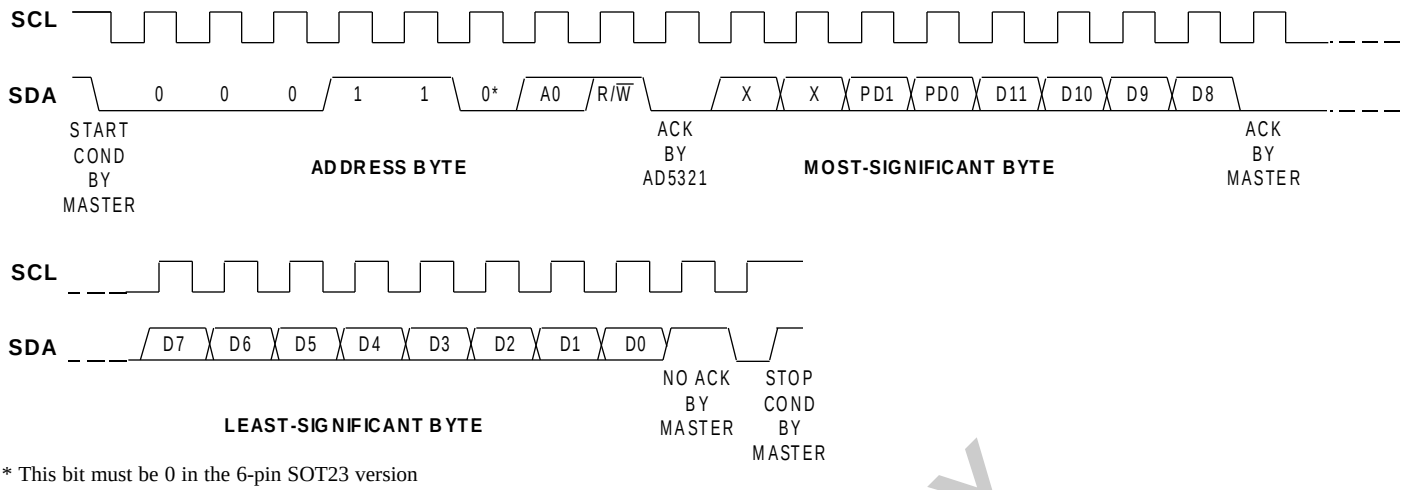
* This bit must be 0 in the 6-pin SOT23 version

AD5311 READBACK SEQUENCE



* This bit must be 0 in the 6-pin SOT23 version

AD5321 READBACK SEQUENCE

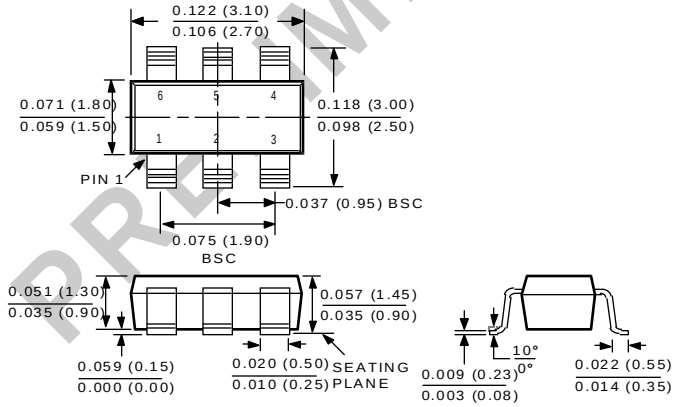


* This bit must be 0 in the 6-pin SOT23 version

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead SOT-23 (RT-6)



8-Lead MicroSOIC (RM-8)